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a p-type well formed in the substrate for the NMOS transistor and an n-type well formed in the substrate for the PMOS transistor, the p-type and n-type wells being isolated from one another; and

respective contact portions for applying to the semiconductor substrate via the wells different bias voltages in a transistor operating state and a transistor standby state so that active regions of the different conductivity type transistors are fully depleted simultaneously in the standby state.

REMARKS

This is in response to the office Action dated August 6, 2002. Claims 22 and 23 have been canceled (and their respective subject matter added to claims 1 and 7). Thus, claims 1, 4-11 and 24 are now pending. Attached hereto is a marked-up version of the changes made to the claim(s) by the current amendment. The attached page(s) is captioned "**Version With Markings To Show Changes Made.**"

No new issues are presented herein. The only claim amendments herein are for: (1) addressing Section 112 issues; and (2) incorporating subject matter of claims 22 and 23 into claims 1 and 7, respectively. Thus, no new issues are presented herein, and no new search is needed. This Amendment should be entered.

As a housekeeping matter, it is respectfully requested that the Examiner confirm consideration of the IDS filed August 19, 2002.

Claims 22-24 stand objected to in paragraph 2 of the Office Action, and claims 5, 6, 9 and 10 stand rejected under 35 U.S.C. Section 112, second paragraph, in paragraph 4

of the Office Action. It is respectfully submitted that the claim changes herein address and overcome any potential issue(s) in this regard.

Claim 1 stands rejected under 35 U.S.C. Section 103(a) as being allegedly unpatentable over Burr in view of both Numata and Yamaguchi. This Section 103(a) rejection is respectfully traversed for at least the following reasons.

Claim 1 requires ". . . . transistor including *source and drain regions of a second conductivity type*, a channel of the first conductivity type, and wherein an *impurity diffusion layer of the first conductivity type is formed in the semiconductor substrate under at least the entire source, drain and channel regions*, so that the impurity diffusion layer is of the same conductivity type as the semiconductor substrate . . . . contact hole reaching the impurity diffusion layer so that the different bias voltages are applied to the substrate via the impurity diffusion layer; and a second MOS transistor, wherein the *first and second MOS transistors are of different conductivity types on the substrate, and wherein bias voltage for both of the transistors is changed between the active and standby states so that active regions of the transistors are fully depleted simultaneously in the standby state*." For example, see Fig. 3 of the instant application which illustrates that the source/drain (S/D) regions 36 are n-type and the impurity diffusion layer 31a under at least the entire S/D and channel regions is p-type. Thus, claim 1 clearly requires that the impurity diffusion layer and the S/D regions be of *different* conductivity types. Moreover, claim 1 also requires controlling the bias voltage for PMOS and NMOS transistors on the same substrate between the active and standby state(s) so that active

regions of the transistors are *fully depleted simultaneously in the standby state*. The cited art fails to disclose or suggest these aspects of claim 1.

A. The cited art fails to disclose/suggest controlling the bias voltage for PMOS and NMOS transistors so that active regions of the transistors are *fully depleted simultaneously in the standby state* as required by claim 1

Burr, Numata and Yamaguchi all fail to disclose or suggest controlling the bias voltage for PMOS and NMOS transistors on the same substrate between the active and standby state(s) so that active regions of the transistors are *fully depleted simultaneously in the standby state*. Thus, even the alleged Section 103(a) combination fails to meet this aspect of claim 1. In particular, the Office Action admits that Burr and Numata fail to disclose or suggest this aspect of claim 1. Recognizing this deficiency in Burr and Numata, the Office Action cites to Yamaguchi.

Yamaguchi discloses changing a bias voltage between the standby state and the active state. However, as shown in Fig. 15 of Yamaguchi, the threshold voltage and the current supplying drivability can be changed by fully depleting one of the transistors (NMOS), but the other transistor (PMOS) cannot be fully depleted at the same time. Accordingly, it can be seen that none of the three (3) cited references discloses or suggests controlling the bias voltage for PMOS and NMOS transistors on the same substrate between the active and standby state(s) so that active regions of the transistors are *fully depleted simultaneously in the standby state*. Thus, even if the three references were combined as alleged in the Office Action (which applicant believes would be incorrect in any event), the invention of claim 1 still would not be met.

B. <u>The Section 103 combination of Burr/Numata is legally flawed re claim 1</u>

Claim 1 requires that the impurity diffusion layer and the S/D regions be of *different* conductivity types, and that the contact hole reaches the impurity diffusion layer so that the different bias voltages are applied to the substrate via the impurity diffusion layer. The Office Action admits that Burr fails to disclose or suggest this aspect of claim 1, and thus cites to Fig. 20 of Numata. The Office Action apparently contends that it would have been obvious to one of ordinary skill in the art to have used the contact connection of Fig. 20 of Numata in order to contact the well of Burr. The Section 103(a) combination of Burr and Fig. 20 of Numata is fundamentally flawed and legally incorrect.

Burr discloses a diffusion layer (e.g., well 750) and source/drain regions (e.g., 712, 714) of *different* conductivity types. However, given these different conductivity types, Burr repeatedly states that the diffusion layer must be aligned directly under only the intrinsic channel region (i.e., diffusion layer cannot extend outside of the S/D regions) (e.g., col. 5, lines 54-56; col. 7, lines 18-20). Thus, Burr requires a well contact from the substrate side (not the transistor side) which is directly contrary to the invention of claim 1. Recognizing that Burr fails to disclose or suggest the diffusion layer contact arrangement required by claim 1, and that it cannot accommodate the same since Burr's well does not extend past the periphery of the channel, the Office Action cites to Numata.

Numata in Fig. 20 discloses an expanded back gate 11 which extends past the channel and source/drain regions so that a contact 19 can be made from the transistor side

of the substrate. However, the only reason that Numata can extend its back gate 11 past the channel and source/drain regions to enable contact 19 is because the back gate 11 is always of the *same* conductivity type as the source/drain. When the Fig. 20 embodiment of Numata is applied to an n-type MOSFET, both the back gate 11 and source/drain regions 7 are n-type (e.g., col. 8, lines 4 and 38-41; and col. 16, lines 25-29 and 39-41); whereas when the Fig. 20 embodiment is applied to a p-type MOSFET both the back gate 11 and the source/drain regions are p-type (e.g., col. 17, line 65; and col. 18, lines 19-35). In Numata, since the back gate 11 and source/drain regions 7 have the same conductivity type in Numata, the back gate 11 can be expanded without adversely affecting transistor operation according to Numata.

However, there is no suggestion in the art of record that would have caused one of ordinary skill in the art to have expanded a diffusion layer as required by claim 1 so as to be located under at least the channel and source/drain regions in a situation where the diffusion layer is of a *different* conductivity type that the source/drain regions. In contrast, Burr teaches that this should not be done. Accordingly, the Section 103(a) combination of Burr and Numata in the Office Action is fundamentally flawed and incorrect.

C. Claims 7 and 24

Independent claims 7 and 24 also require controlling the bias voltage for PMOS and NMOS transistors on the same substrate between the active and standby state(s) so that active regions of the transistors are *fully depleted simultaneously in the standby state*. As explained above, none of the three cited references disclose or suggest this aspect of

claims 7 and 24. Thus, even the alleged Section 103(a) combination fails to meet this aspect of claims 7 and 24.

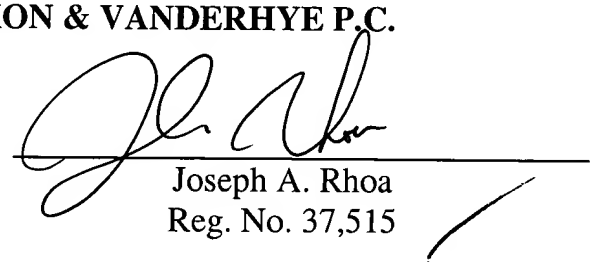
Additionally, the Section 103(a) combination of Burr and Numata is fundamentally flawed for the reasons discussed above. Again, the rejection of claims 7 and 24 should be withdrawn.

D. Conclusion

For at least the foregoing reasons, it is respectfully requested that all rejections be withdrawn. All claims are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: 

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please cancel claims 22-23.

1. (*Amended*) A semiconductor device comprising:

a first MOS transistor formed on a semiconductor layer of an SOI substrate in which the semiconductor layer is formed on a semiconductor substrate of a first conductivity type with the intervention of a buried insulating film,

a contact portion for applying to the semiconductor substrate different bias voltages in an operating state and a standby state of a semiconductor circuit including the MOS transistor,

the transistor including source and drain regions of a second conductivity type, a channel of the first conductivity type, and wherein an impurity diffusion layer of the first conductivity type is formed in the semiconductor substrate under at least the entire source, drain and channel regions, so that the impurity diffusion layer is of the same conductivity type as the semiconductor substrate, [and]

wherein the contact portion for applying the different bias voltages is formed in a device isolation region and comprises a contact hole in the semiconductor layer and the buried insulating film, said contact hole reaching the impurity diffusion layer so that the different bias voltages are applied to the substrate via the impurity diffusion layer[.]; and

a second MOS transistor, wherein the first and second MOS transistors are of different conductivity types on the substrate, and wherein bias voltage for both of the

transistors is changed between the active and standby states so that active regions of the transistors are fully depleted simultaneously in the standby state.

4. (*Amended*) A semiconductor device according to claim 1, wherein the impurity diffusion region is formed as a well in a surface of the semiconductor substrate which lies under the first MOS transistor, the well having an impurity concentration higher than that of the other region of the substrate, and the bias voltages are applied to the well.

5. (*Amended*) A semiconductor device according to claim 4, wherein the well is a P-type well under an N-channel MOS transistor which is the first of said MOS transistors, while [the] a well for the other of the MOS transistors is an N-type well under a P-channel MOS transistor which is the second of said MOS transistors.

6. (*Amended*) A semiconductor device according to claim 5, wherein a plurality of wells including the P-type well and the N-type well are formed in the semiconductor substrate and the P-type well and the N-type well are substantially electrically isolated from each other.

7. (*Amended*) A semiconductor device comprising:

a first MOS transistor formed on a semiconductor layer of an SOI substrate in which the semiconductor layer is formed on a semiconductor substrate with the intervention of a buried insulating film,

an element isolating region formed in the semiconductor layer, [and]

a contact region formed in the element isolating region for connection with a contact portion for applying a bias voltage to a well of the semiconductor substrate, the well being of the first conductivity type as is the other region of the semiconductor substrate directly under the well[.]; and

a second MOS transistor, wherein the first and second MOS transistors are of different conductivity types on the substrate, and wherein bias voltage for both of the transistors is changed between the active and standby states so that active regions of the transistors are fully depleted simultaneously in the standby state.

8. (*Amended*) A semiconductor device according to claim 7, wherein the well is formed in a surface of the semiconductor substrate which lies under the first MOS transistor formed on the semiconductor layer, the well having an impurity concentration higher than that of the other region of the substrate, and the bias voltages are applied to the well.

9. (*Amended*) A semiconductor device according to claim 8, wherein the well is a P-type well under an N-channel MOS transistor which is the first of said MOS transistors, while [the] a well for the other of the MOS transistors is an N-type well under a P-channel MOS transistor which is the second of said MOS transistors.

24. (*Amended*) A semiconductor device comprising:

a PMOS transistor and an NMOS transistor formed on a semiconductor layer of an SOI substrate in which the semiconductor layer is formed on a semiconductor substrate of a first conductivity type with the intervention of a buried insulating film,

a p-type well formed in the substrate for the NMOS transistor and an n-type well formed in the substrate for the PMOS transistor, the p-type and n-type wells being isolated from one another; and

respective contact portions for applying to the semiconductor substrate via the wells different bias voltages in a transistor operating state and a transistor standby state so that active regions of the different conductivity type transistors are fully depleted simultaneously in the standby state.